RAPIDO'15, 7th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools

An Efficient Joint Analytical and Simulation-based Design Space Exploration Flow for Predictable Multi-Core Systems

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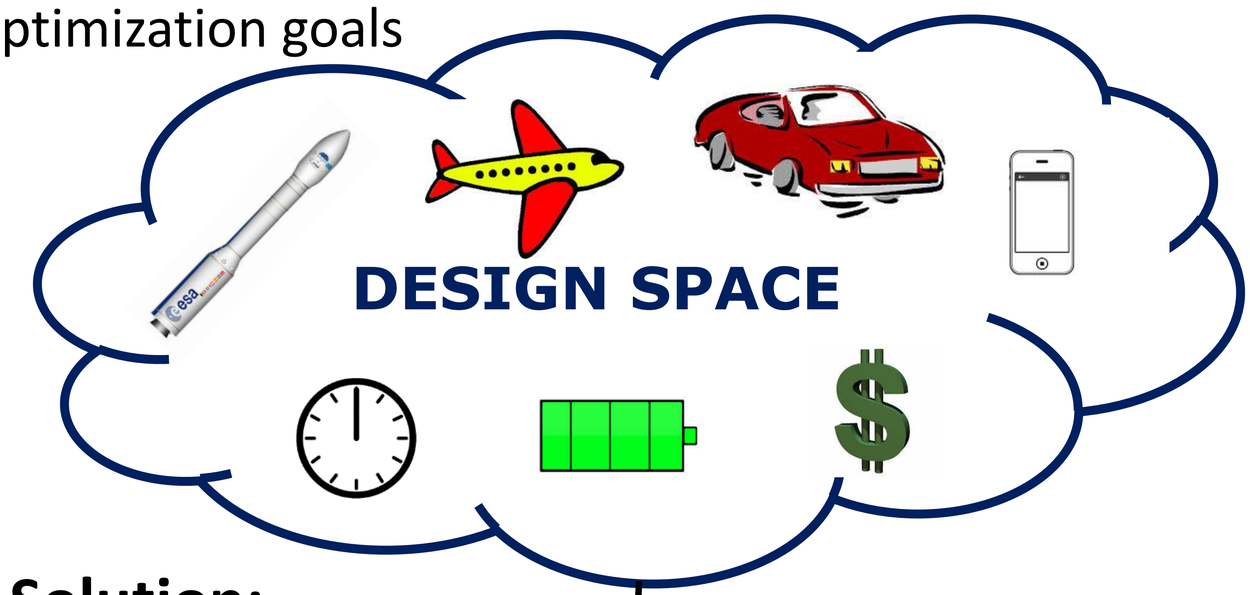
Goal:

Faster and **More Efficient design** of Time Critical and Mixed-Criticality Systems

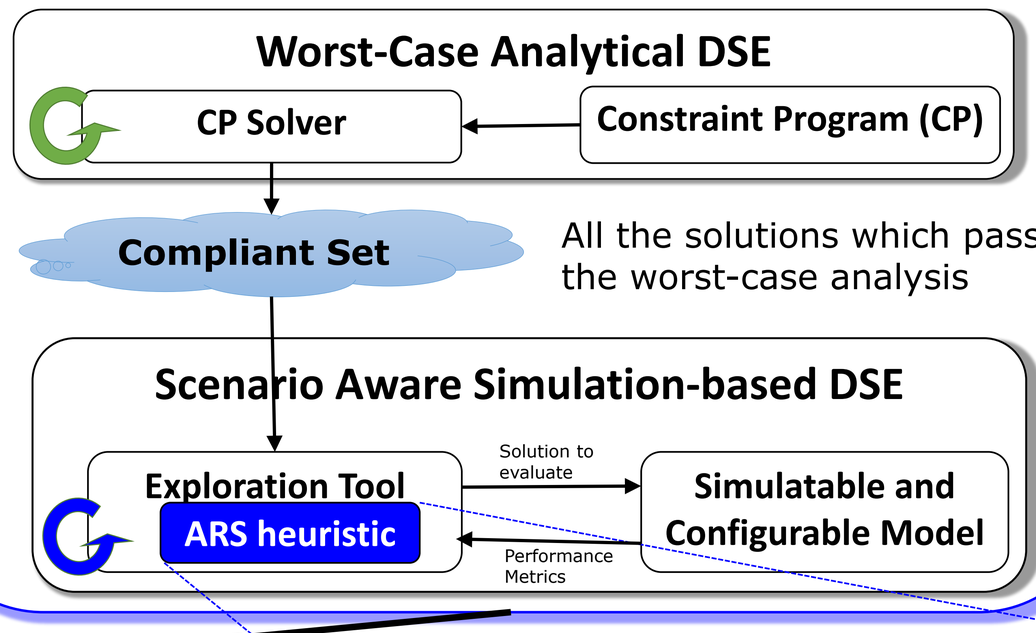
Challenge:

Huge design space, critical time constrains and optimization goals



Solution:

Joint Analytical and Simulation-based DSE



Pareto Set

Adaptive Random Sampling

Enables heuristic search both in Analytical and Simulation-based DSE

Results:

Significantly Faster Design Time

Table 4: Number of solutions found by A-DSE and DSE time for different configurations of the system bus and design constraints

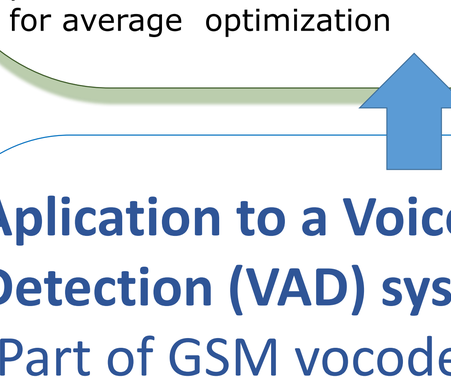
Design case	CONF1 # Solut.	CONF1 Runtime	CONF2 # Solut.	CONF2 Runtime
unconstr.	1089946	34min.27s	2234194	1h (*)
C_m	68200	4min. 6s	2119553	1h (*)
$C_m \wedge C_s(3)$	50025	3min. 52s	187316	8min 14s
$C_m \wedge C_s(1)$	1129	2min.	1129	2min.

Simulation-base exploration would take weeks!

90% Cut of Original Design Space through the Analytical DSE in minutes

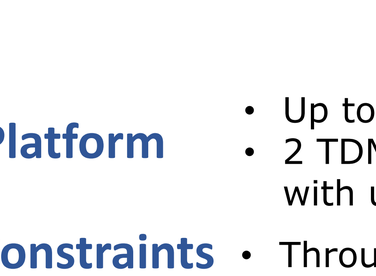
It would still take 14h!

ARS heuristic enables saving 80% of the simulations wit a negligible impact in the search of the Pareto Set

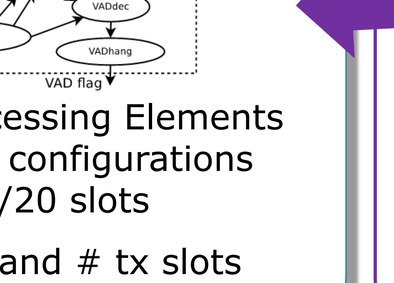


More efficient Designs

- New solutions revealed after JAS-DSE vs A-DSE (>30%, conf1: 11 out of 32, conf2: 14 out of 36)
- Thousands of solutions dissapear as optimum ones



Worst-case analysis prevents accurate decisions for average optimization

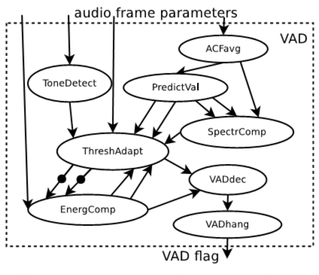


Avg. Cycle <50μs ⇒ 3PEs, and not 4 PES, are required

Aplication to a Voice Activity Detection (VAD) system

(Part of GSM vocoder)

Application

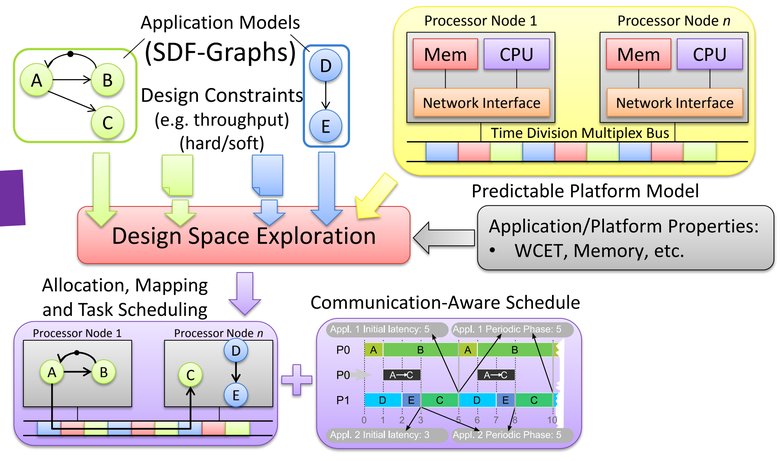


Platform
- Up to 6 Processing Elements
- 2 TDMA bus configurations with up to 8/20 slots

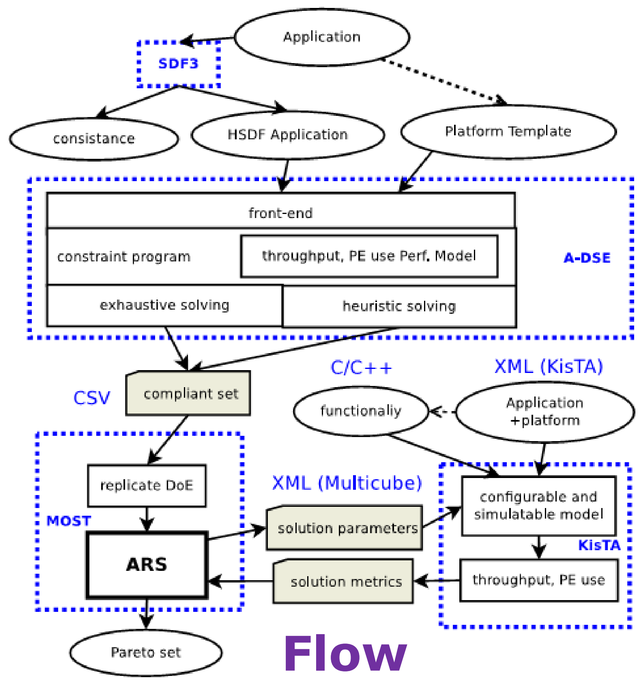
Constraints
- Throughput and # tx slots

Goals
- Throughput, Avg. Load, #PEs

Implementation for Predictable MPSoC Design



Input Model



Flow

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